

What is claimed is:

- 1    1. A method for modifying the function of a state machine having a programmable logic  
2    device, the method comprising:  
3        (a) modifying a high-level design of said state machine to obtain a modified high-  
4    level design of said state machine with a modified function;  
5        (b) generating a programmable logic device netlist from differences in said high-  
6    level design and said modified design; and  
7        (c) installing said modified function into said state machine by programming said  
8    programmable logic device based on said programmable logic device netlist.

- 1    2. The method of claim 1, wherein step (b) includes:  
2        extracting a high-level programmable logic device design from said modified  
3    high-level design.

- 1    3. The method of claim 2, wherein said extracting includes comparing said high-level  
2    design to said modified high-level design.

- 1    4. The method of claim 2, wherein said generating a programmable logic device netlist  
2    includes synthesizing said a high-level programmable logic device design.

1 5. The method of claim 4, wherein said programming of said programmable logic device  
2 includes compiling said programmable logic device into a pattern and applying said  
3 pattern to a static random access memory array of an integrated circuit containing said  
4 state machine and said programmable logic device.

1 6. The method of claim 1, further including the step of:  
2 (d) determining if said programmable logic device includes enough gates to  
3 program said modified function.

1 7. The method of claim 1, further including, before step (a) performing a static timing  
2 analysis to determine a maximum allowable size for said programmable logic device.

1 8. The method of claim 6, wherein said performing said static timing analysis is  
2 performed on a netlist synthesized from said high-level design of said state machine.

1 9. The method of claim 1, wherein said high-level design of said state machine is a  
2 portion of a high level design of an integrated circuit and said modified high-level design  
3 of said state machine is a portion of a modified version of said high level design of said  
4 integrated circuit.

1 10. The method of claim 1, wherein said high-level design of said state machine includes  
2 one or more multiplexers for interconnecting said programmable logic device to said state  
3 machine.

1 11. The method of claim 1, wherein said programmable logic device is connectable  
2 between a next stage logic and a state latch of said state machine in either a next state  
3 path, a current state path or both.

1 12. The method of claim 1, wherein said programmable logic device is connectable  
2 between an input of said state machine, an output of said state machine or both.

1 13. The method of claim 1, wherein said programmable logic device is adapted to add  
2 programmable logic device latch bits to a state latch of said state machine.

1 14. The method of claim 1, wherein said programmable logic device is shared between  
2 said state machine and one or more additional state machines.

1 15. The method of claim 1, wherein said programmable logic device is selected from the  
2 group consisting of programmable read only memories, simple programmable logic  
3 devices, programmable array logic devices, generic array logic devices, programmable  
4 logic arrays, complex programmable logic devices, erasable programmable logic devices,

- 5 electrically-erasable programmable logic devices, multiple array matrices, field
- 6 programmable interconnect devices, static random access memory based programmable
- 7 logic devices and antifuse based programmable logic devices.

1 16. A computer system comprising a processor, an address/data bus coupled to said  
2 processor, and a computer-readable memory unit adapted to be coupled to said processor,  
3 said memory unit containing instructions that when executed by said processor implement  
4 a method for modifying the function of a state machine having a programmable logic  
5 device, said method comprising the computer implemented steps of:  
6 (a) modifying a high-level design of said state machine to obtain a modified high-  
7 level design of said state machine with a modified function;  
8 (b) generating a programmable logic device netlist from differences in said high-  
9 level design and said modified design; and  
10 (c) installing said modified function into said state machine by programming said  
11 programmable logic device based on said programmable logic device netlist.

1 17. The system of claim 16, wherein step (b) includes:  
2 extracting a high-level programmable logic device design from said modified  
3 high-level design.

1 18. The system of claim 17, wherein said extracting includes comparing said high-level  
2 design to said modified high-level design.

1 19. The system of claim 17, wherein said generating a programmable logic device netlist  
2 includes synthesizing said a high-level programmable logic device design.

1 20. The system of claim 19, wherein said programming of said programmable logic  
2 device includes compiling said programmable logic device into a pattern and applying  
3 said pattern to a static random access memory array of an integrated circuit containing  
4 said state machine and said programmable logic device.

1 21. The system of claim 16, further including the step of:  
2 (d) determining if said programmable logic device includes enough gates to  
3 program said modified function.

1 22. The system of claim 16, further including, before step (a) performing a static timing  
2 analysis to determine a maximum allowable size for said programmable logic device.

1 23. The system of claim 21, wherein said performing said static timing analysis is  
2 performed on a netlist synthesized from said high-level design of said state machine.

1 24. The system of claim 16, wherein said high-level design of said state machine is a  
2 portion of a high level design of an integrated circuit and said modified high-level design  
3 of said state machine is a portion of a modified version of said high level design of said  
4 integrated circuit.

1 25. The system of claim 16, wherein said high-level design of said state machine includes  
2 one or more multiplexers for interconnecting said programmable logic device to said state  
3 machine.

1 26. The system of claim 16, wherein said programmable logic device is connectable  
2 between a next stage logic and a state latch of said state machine in either a next state  
3 path, a current state path or both.

1 27. The system of claim 16, wherein said programmable logic device is connectable  
2 between an input of said state machine, an output of said state machine or both.

1 28. The system of claim 16, wherein said programmable logic device is adapted to add  
2 programmable logic device latch bits to a state latch of said state machine.

1 29. The system of claim 16, wherein said programmable logic device is shared between  
2 said state machine and one or more additional state machines.

1 30. The system of claim 16, wherein said programmable logic device is selected from the  
2 group consisting of programmable read only memories, simple programmable logic  
3 devices, programmable array logic devices, generic array logic devices, programmable  
4 logic arrays, complex programmable logic devices, erasable programmable logic devices,

- 5 electrically-erasable programmable logic devices, multiple array matrices, field
- 6 programmable interconnect devices, static random access memory based programmable
- 7 logic devices and antifuse based programmable logic devices.